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Performance Evaluation of MOSFET against CNTFET and GNRFET

Rakesh Yadav Manjunath[1*] and Pallavi Venkatesh[1]

1. Department of Computer Engineering, California State University, Fullerton, USA.

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*Corresponding Author: R. Y.Manjunath (rakesh1991@csu.fullerton.edu)

Abstract
As the CMOS technology is being scaled down further into the nanoscale, we are witnessing lot of short channel effects which are resulting in considerable deviation from its normal behavior. Also, the leakage current is increasing which is leading to power dissipation issues is small chips. Because of this many alternative technologies are being explored with an intent to replace the existing CMOS technology. Carbon Nanotube Field Effect Transistor (CNTFET) and Graphene Nanoribbon Field Effect Transistor (GNRFET) are among the technologies which are being widely studied and has been proposed to be a likely candidate to replace the MOSFET technology. In this paper, we have done extensive simulations on CNTFET and GNRFET, looking at how some of the device parameters affects the performance of the CNTFET and GNRFET. We have used the HSPICE and CosmosScope tools for the simulation and verifying the graphs. The CNTFET simulations were done using the model developed by the Stanford University and the GNRFET simulations using the HSPICE model developed by the University of Illinois. The next part of our research was concentrated on comparing the CNTFET and GNRFET with the MOSFET technology. The MOSFET technology was simulated by using the PTM models developed by the Arizona State University. Basic gate like inverter, NAND, NOR and XOR were built using all the three technologies for channel lengths 7nm, 10nm, 16nm and 32nm. The HSPICE and Cosmoscope were then used to find average dynamic power, delay, leakage powers, EDP and PDP in each case to compare between the different technologies. The results showed us that the CNTFET and GNRFET offers reduced power consumption when compared to the MOSFET and also operates at higher speed.

Keywords :MOSFET, CNTFET, GNRFET, HSPICE, PDP

1. Introduction

In the past two decades, an applied technology called Nano electronics has been emerged. CNTFET [3] model that its structure is from carbon can take the place of the old structure of silicon. Since CNTFET model includes the parameters such as the higher power of switch, curves with more ideal voltage, the distribution of carbon transfer speed and better mobility, then, it can be a viable alternative to circuits. It can also be used in integrated circuits and it can cause the lower voltage, which results in lower power consumption and thereby improve its performance in comparison to MOSFET [1]. GNRFET [6] model due to its extraordinary properties in electrical conductivity, high density and mobility of charge carriers, optical conductivity and mechanical properties, it changed to a unique transistor. This transistor has been considered as a suitable candidate to replace silicon in the next generation of photonic and electronic components due to these excellent properties. Photonics is a science that its scope includes publication, transmission, modulation, switching, amplification and detection of light.

CNTFET model compared with MOSFET model is more resistant to high temperatures. So, using

CNTFET, at high temperature we can achieve more speed and less leakage. This paper, at first discuss the structure of the transistors of CNTFET, GNRFET and MOSFET in terms of geometry, manufacturing methods and implementation as well as performance and theory of flow, then the transistors are assessed from channel length and flow rate. The overall structure of the paper organized as follows: In the Section 2, material methods are explained in conjunction with CNTFET, GNRFET, and MOSFET. In the Section 3, simulations and results will be described and finally in the Section 4, conclusion and future works will be explained.

2. Material and Methods

2.1. MOSFET

Metal oxide semiconductor field effect transistor (MOSFET) [1] is a three-terminal device – gate, source and drain uses bulk silicon as the channel. The source and drain regions are formed by process called impact ionization. During the fabrication, a semiconductor either P type or N type is taken and other type of with high impurity concentration is continuously bombarded to give either N-type or P-type MOSFET.

The MOSFET mainly operates in three different regions, namely Cutoff, Linear or Triode region and Saturation region. In cutoff region, the applied drain to source voltage is not strong enough for conduction of current and hence the device will be in off state. Once the applied drain to source voltage is increased beyond a point called threshold, the device starts conducting and there will be a sharp increase in the current (Id) for any increase in the voltage across drain to source (Vds). The last region of operation is called the saturation region, where any further increase in the voltage Vds will have very little effect on the current. At this stage the transistor is said to be in the ON state. The transistor can work as a switch only if enough gate voltage is applied.

Depending on whether N+ region or P+ region are used for forming source and drain regions, there are 2 types of MOSFET's i.e., NMOS and PMOS. In an NMOS transistor the body will be p type semiconductor in which N+ regions are implanted as shown in Figure (1). The NMOS conducts for a gate voltage of logic "1" and the NMOS transistors are good at passing a strong logic 0. In a PMOS transistor the body will be an n type semiconductor in which P+ regions are implanted. The PMOS transistors conducts for a gate voltage of logic "0" and the PMOS transistors are good at passing a strong 1.

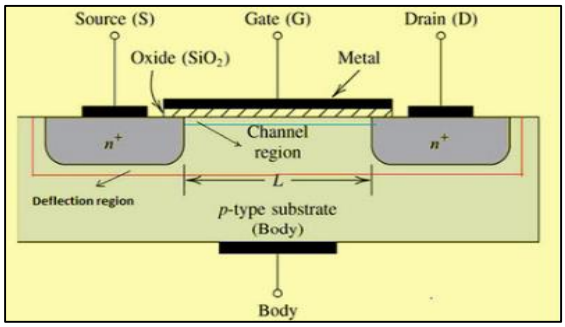


Figure 1: Structure of PMOS Transistors

According to Moore's law the transistor density on a chip doubles every 18 to 24 months. This is done in order to increase speed and also to accommodate more transistors so that a greater performance can be achieved. But as we scale down the devices we are witnessing many phenomenon which are affecting the behavior of the MOSFET. These effects are commonly called as short channel effects. Some of short channel effects are Drain induced barrier lowering (DIBL), Gate induced drain leakage (GIDL), hot carrier effect, gate leakage and others. Due to this short channel effects, the leakage current is increasing which leads to excessive heat dissipation, this affects the overall performance of the chip. To overcome this there have been some new advanced MOSFET structure that are introduced like Silicon on Insulator FET, FinFET, Double gate MOSFET, Ultrathin – Body MOSFET. These newer technologies can suppress the short channel effect to an extent but are not a permanent solution and are not viable for long term scaling. Because of this we are looking at alternative technologies that can replace the MOSFET. CNTFET and GNRFET are among the potential technologies that can replace the MOSFET.

2.2. CNTFET

Carbon nanotubes are a new form of carbon; these are formed by folding graphite layers into carbon cylinders forming a tube-like structure. These tubes have unique properties depending on the folding angle. It is this chirality that makes the carbon nanotubes either metallic or semiconducting, the semiconducting tubes are used in the transistors. These tubes are used instead of bulk silicon for the channel as in the typical silicon MOSFET.

Either a single CNT or an array of CNT's are used to form a channel between the source and the drain. These CNT have a diameter of 1-2nm and are few micro meters in length. Therefore, making the CNT a 1-D transporter of electrons from source to drain. The advantages of

CNTFET are that they have high trans conductance when compared to the MOSFET and also a high Ion to Ioff ratio. This can be credited to the single dimension transport of electron from source to drain. And also, the operating power of the device is less as less gate voltage is required to turn on or turn off the device.

Yet the manufacture process of CNTFET [3] is still difficult as controlling the chirality during the manufacturing process is not easy and any changes in chirality will produce metallic CNTs which then cannot be used as in transistors as it cannot be controlled. The CNT also suffer from reliability issue when they are exposed to a varied temperatures or high electric fields. The CNT's also have less life time as they undergo degradation when exposed to oxygen. In Figure (2) is shown structure of CNTFET.

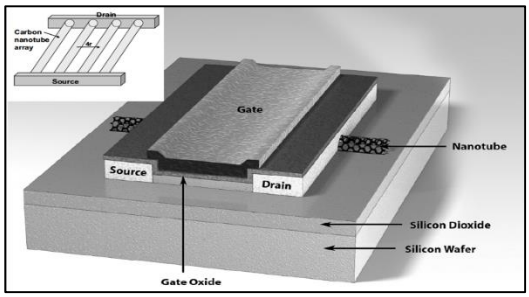


Figure 2: Structure of CNTFET [2]

There are many ways of fabricating a CNTFET like a wrap-around gate CNTFET, bottom gate CNTFET and top gated CNTFET. The top gated CNTFET [3], in which the nanotubes are deposited on the silicon substrate and then using a high-resolution electron beam the surroundings of the nanotube are etched off and a high temperature is used to establish better contacts with the CNT and source/drain regions. A thin layer of dielectric is then deposited on top of it and then the gate. This technique allows for the device to be operated in low powers as the device can be switched at smaller gate voltages.

2.2.1. Properties of CNTFET

Let us now look at some of the device properties of the CNTFET and how they affect the performance.

Diameter: The CNTFET are made by cutting the graphene sheet at a particular angle and then rolling up to make it a hollow cylinder. The usual diameter of the CNT is in the range of 1-2nm.

The simulations (Figure (3)) were done by forming a NAND gate using CNTFET with a channel length of 10nm. The CNTFET had 3 tubes, was supplied with a Vdd of 0.9v and the delay was measured between the 50% of the rise and fall times.

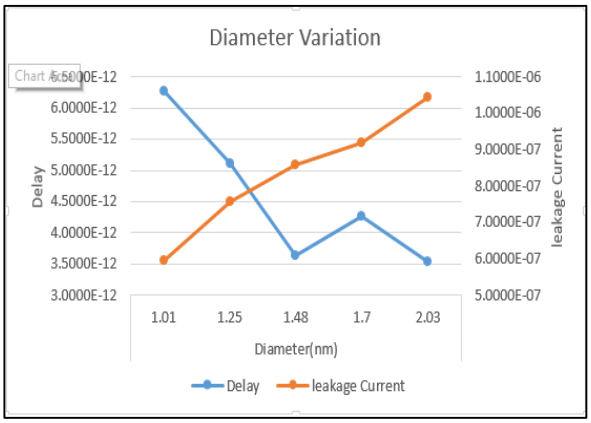


Figure 3: Comparison of graph diameter variation

The chirality in a CNTFET plays a very important role. The chirality can be changed in the carbon nanotube model by changing the n1 and n2 values in the parameter list.

Equation (1) is the relation between chirality and the diameter.

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \quad (1)$$

Where (a) is the length between 2 carbon atoms, which is approximately equal to 1.42A0.

$$E_G = +E(k) - \{-E(k)\} = 2.\frac{3ta_{c-c}}{2}\sqrt{\left(\frac{2}{3d}\right)^2} \quad (2)$$

$$= \frac{2a_{c-c}t}{d} = \frac{0.8}{d}[ev/nm]$$

The Equation (2) show the relation between the energy band gap and the diameter (d). E_g is inversely proportional to the diameter that means as we increase the diameter the energy band gap decreases.

$$V_{th} \approx \frac{E_g}{2e} \quad (3)$$

The Equation (3) relates energy band and the threshold voltage of a CNTFET. Where e is the electron charge which is a constant. Therefore, the threshold voltage is directly proportional to the Energy band gap Eg. In other words, as we increase the diameter the threshold voltage decreases.

The smaller the delay the faster the CNTFET operates that means as we reduce the Vth the device need less voltage to turn on. But the other effect of reduced Vth is that the leakage power increases. Both these are shown in the Figure (3).

Number of Carbon Nanotubes: Multiple carbon nanotubes can be placed between the source and drain. By doing this we can achieve better speed. Figure (4) that shows multiple nanotubes placed between common source and drain.

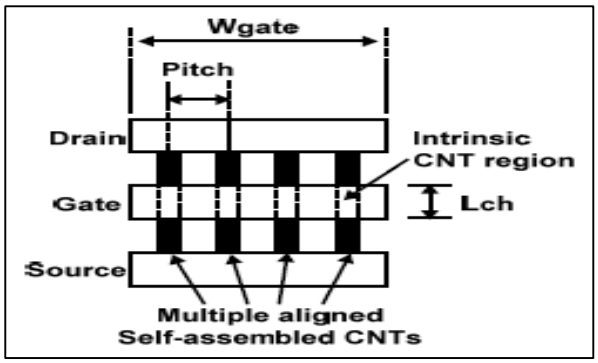


Figure 4: CNTFET with multiple CNTs [4]

The maximum number of tubes that can be placed depends on the width of the source or drain regions. The following simulations was performed for a CNT length of 32nm and a supply voltage of 0.9V was maintained. The inverter gate delay was measured at 50% of the output voltage to the 50% of the input.

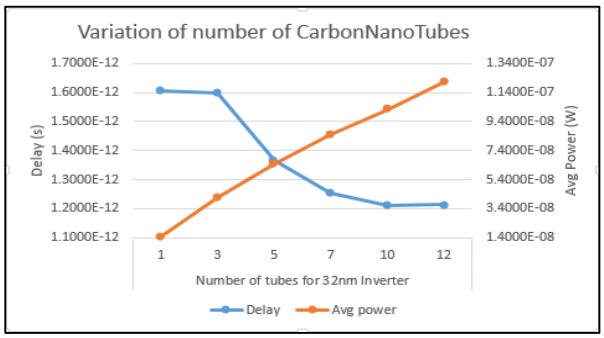


Figure 5: Graph of delay and average dynamic power vs number of carbon nanotubes

As we can see from the Figure (5) as we increase the number of tubes from 1 to 12 the delay is decreasing but on the contrary as we increase the number of tubes the power consumed in the device will be more since there will be more current flow every time the transistor is either switched ON or switched OFF. Also, there is a decrease in delay, till we increase the number of tubes to 10 beyond which the delay saturates, any further increase in the number of tubes will only lead to increase in the power. The other aspect which we need to consider is how closely these tubes can be packed, this is given by the pitch.

Pitch: pitch is defined as the distance between the centers of two adjacent CNTs in the same device [5] as shown in Figure 2. The simulations (Figure (6)) were performed using a CNTFET with 3 nanotubes each with length of 10nm. A NAND gate was built using this FET and supply voltage of 0.9V was given. The delay was measured between the time taken for the output to reach 50% of Vdd once the input has reached 50% of supply.

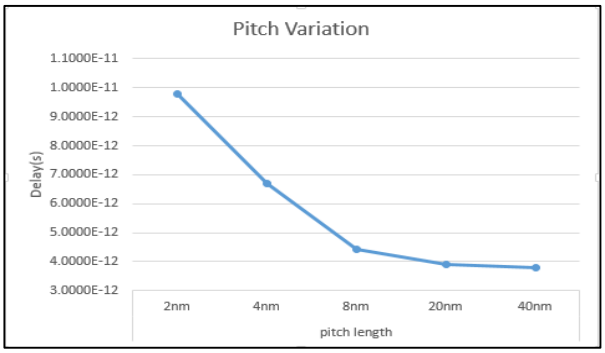


Figure 6: Graph of Pitch Variation Vs Delay

As the pitch decreases the carbon nanotubes are brought closer to each other, this increases the total channel capacitance and also the overall current in the CNTFET will be reduced due to screening effect [5]. Screening effect is the force of repulsion between the electrons.

Looking at the graph in Figure 6, as we increase the pitch the delay decreases but when the tubes are brought closer to each other in other words when pitch is decreased, the current reduces this in turn reduces the speed of operation of the device.

Therefore, while using CNTFET it is important to understand how the various parameter affect the performance of the transistor. The best results can be obtained by using multiple tubes that are placed farther from each other, this means we have to use a wider channel and also choosing the right diameter of the CNTFET is also important as this will affect both speed and the power.

2.3. GNRFET

Graphene a carbon material formed by a two-dimensional honey comb lattice has shown lot of good electrical, thermal and physical properties which is why this is being studied widely. A graphene sheet does not have any energy band gap which makes it a semi metal like material. However, when a strip of graphene is cut to make a FET out of it shows energy band gap between the top most valence band and bottom most conduction band. Unlike the carbon nanotube which is difficult to make as it requires the graphene to be cut in certain angle and length, the graphene nanoribbon (GNR) on the other will be mostly semiconductor in nature when cut Figure (7) 10nm due to the edge effect [6].

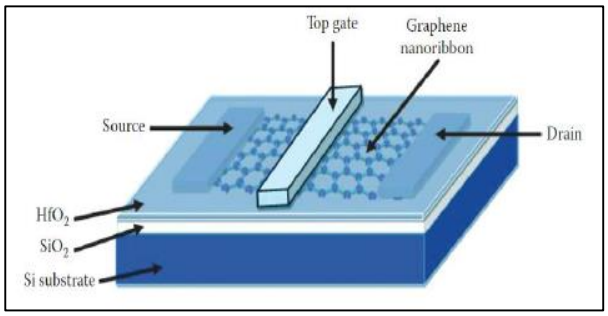


Figure 7: Top Gated GNRFET

There are two type of GNRFETs a schottky barrier (SB) GNRFET and MOS like GNRFET like the one show in Figure 7. The SB type uses metal to form contacts and thereby avoiding the necessary for additional doping [7, 8]. But the SB type GNRFETs offer much less Ion to Ioff ratio when compared to the MOS type GNRFETs [9]

The GNRs are ultrathin layers of graphene these support 1-D ballistic transport of electrons, however there are lot of challenges still to be met like any variations in this structure of GNR can have a large impact on the performance of the device.

2.3.1. Properties of GNRFET:

Width of GNR: The width of the GNR is nothing but the circumference when compared to the CNT. The GNR is cut from the graphene sheet. In the Figure (8) we can see that multiple graphene nanoribbons can be laid next to each other where the contact with the source or drain region is made along the width of the nanoribbon.

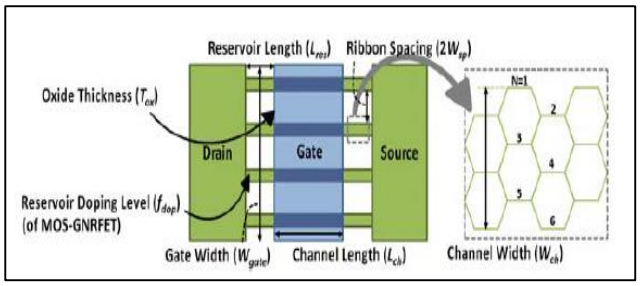


Figure 8. Nanoribbon GNRFET with armchair chirality [10]

The width of GNR is given by Equations (4,5).

$$WAGNR = \sqrt{3}/2 * acc * (N-1) \quad (4)$$

$$WZGNR = 3/2 * acc * (N-1) \quad (5)$$

Where AGNR is the armchair type nanoribbon and ZGNR is the zigzag type GNR, acc is the carbon to carbon bond length which is equal to 1.42A0 and N is the number of dimer lines. Also, the energy band gap in GNR is given by, EG (GNR) = $\frac{0.8\pi}{2W}$ W is the width of the GNR.

Therefore, any increase in the width will reduce the energy band gap and therefore it will mean that less energy is needed for charge carriers to surmount the energy gap to move into conduction band. Therefore, increasing the width should increase on current and decrease delay but increasing width also means that more collisions between charge carriers and this will reduce the ballistic transport or mean free path of carriers and therefor lowers the speed as seen in the Figure (9).

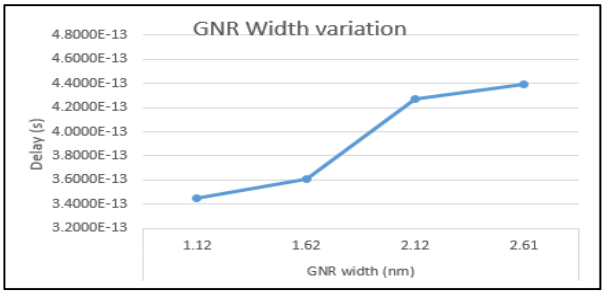


Figure 9. Graph of GNR Width vs Delay.

LER: Line edge roughness occurs when GNRs are cut from the sheet of graphene. These lead to dangling bonds on the edges. Also the width itself may from one end of the GNR to the other end as shown in the Figure 10.

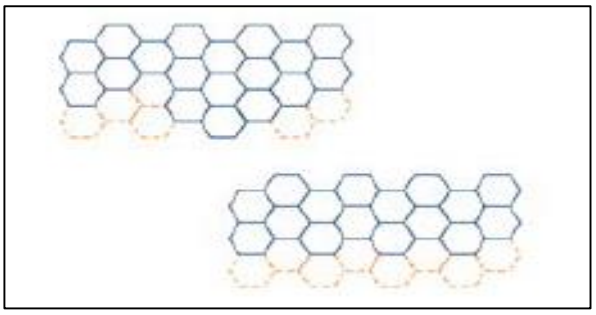


Figure 10. LER in Graphene nanoribbon [10]

The top GNR in the Figure (10) has many dangling bonds and also the width is not uniform as compared to the GNR in the bottom which is more uniform. Presence of dangling bonds lead to scattering of chare carriers and this increase the delay and also the width of the GNR affects the energy band this affects the electrical properties of the GNRFET [9].

Figure (11) is the simulations conducted for an Inverter with GNR length of 10nm and 6 GNRs being placed between source and drain. The LER is varied as percentage of total width.

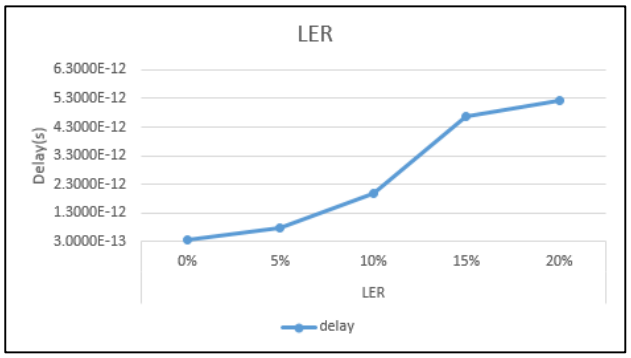


Figure 11. Graph of LER vs Delay

As we see from the Figure (11) as amount of roughness increases the delay also increases. This is one of the main challenges faced by the GNRFET.

Doping Concentration of Source and Drain: Doping is adding impurity atoms to an intrinsic or pure material. The purpose of the doping is to increase the number of free charge carriers that can contribute to the conduction or switching in case of transistors. As we see from the Figure (12) as we increase the doping concentration of source and drain the delay decreases since more electrons or holes can now flow from source to drain. In Figure (12) is shown by increasing the doping concentration of p-type and n-type GNRFET from 0.001 to 0.015 for an inverter with channel length 10nm and supply voltage 0.9v.

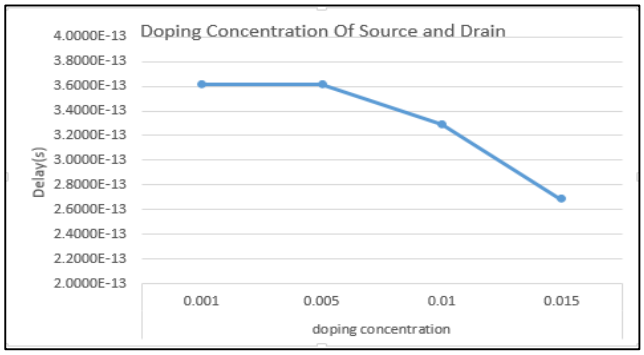


Figure 12: Graph of doping concentration vs Delay

3. Simulations and Results

HSPICE: HSPICE is the industry most popular circuit simulator as it can provide an accurate simulation result. The advantages of using HSPICE are: [11, 12]

- It offers robust 192-bit encryption compliant with Triple Data Encryption Standards (DES) which the netlist provided is kept confidential where the third party can only see the device and the circuit as a black box.
- The transistor level and the Verilog-A which described the analog circuit behavior, can be mixed into a netlist.
- It provides transient noise analysis which enables the users to predict the effect of noise in the device.

CosmosScope: CosmosScope is used to turn the mountain of data into useful information. The feature of CosmosScope such as the powerful analysis and measurement capabilities, patented waveform-calculator technology, and scripting language based on the industry standard Tcl/Tk make it has unparalleled capability and flexibility to analyze design performance and ensure design quality. The advantages of using Cosmos Scope are: [13]

- It supports all Synopsys simulation products such as HSPICE.
- It provides scripting language for easy customization.
- It can perform post-processing of analog and digital simulation results
- The graphs can be annotated automatically with design information.
- The graphs can be saved and stored for further editing.

Basic gates:

The Figure (13) logic gates are constructed using CMOS logic in which there are equal number of NMOS and PMOS transistors [14] complementing each other.

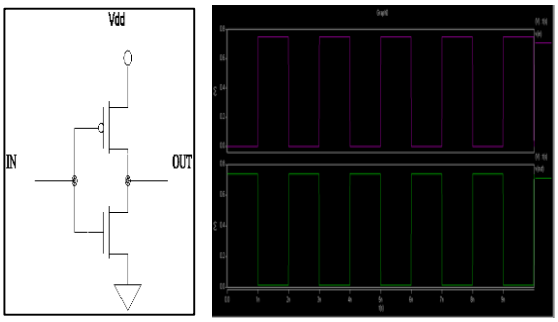


Figure 13.CMOS logic for Inverter and CosmosScope graph for inverter using 10nm channel length MOSFET

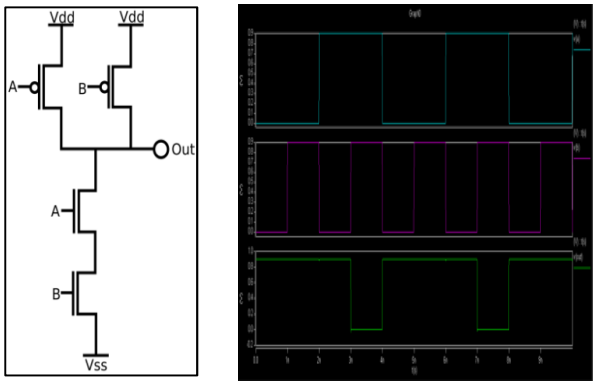


Figure 14. CMOS logic for NAND and CosmosScope graph for NAND using 16nm channel length CNTFET

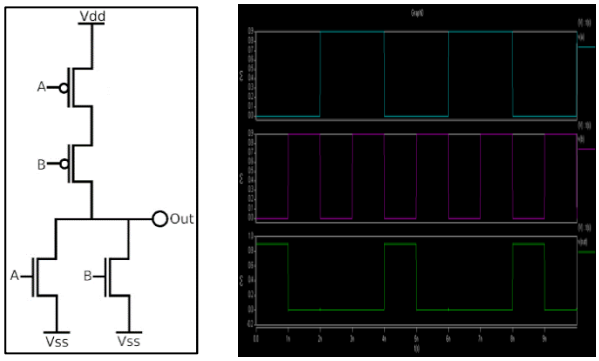


Figure 15. CMOS logic for NOR and CosmosScope graph for NOR using 16nm channel length GNRFET

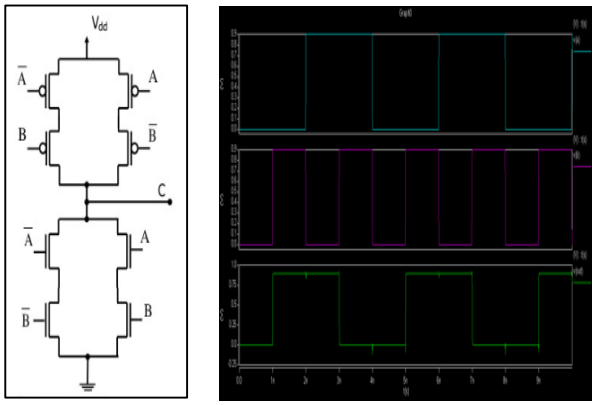


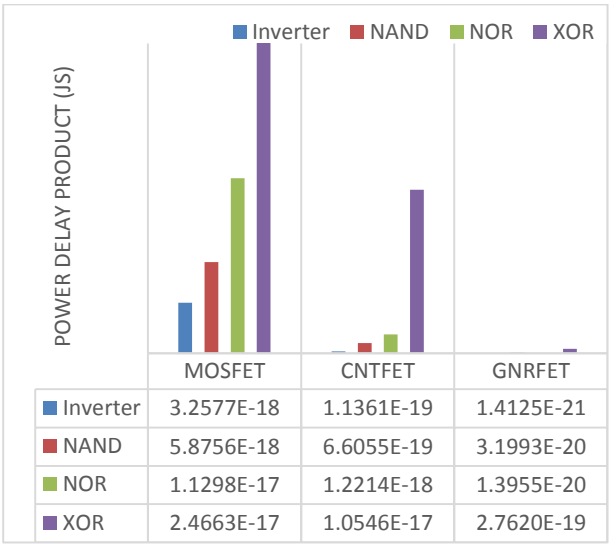
Figure 16. CMOS logic for XOR and CosmosScope graph for XOR using 10nm channel length CNTFET

The MOSFET simulations are performed using predictive technology models from Arizona State University, we have used PTM multi gate HP models which is based on an advanced MOSFET technology - FINFET for 7nm and 10nm channel length and 16nm, 32nm using PTM low power application models. Nominal supply voltage of 1V is used for 32nm, 0.9V for 16nm, 0.75V for 10nm and 0.7V for 7nm channel length. The simulations are run for a period of 50ns, which is also the time used for calculating the dynamic power. The delay is calculated as the time taken once the input has reached 50% of its maximum swing to the time required for the output to reach 50% of its maximum swing. Temperature of 100 C is maintained for all the simulations.

The CNTFET simulations are performed using CNTFET spice compatible model from Stanford University for carbon nanotube lengths of 7nm, 10nm, 16nm and 32nm. Supply voltage of 0.9V is used for all the channel lengths, with diameter of 1.487nm and 3 carbon nanotubes are used as channel with pitch of 20nm. Simulations are performed for a period of 50ns and dynamic power is measured for the same time.

The GNRFET simulations are performed using GNRFET spice compatible model from University of Illinois for the graphene nanoribbon lengths of 7nm, 10nm, 16nm and 32nm. 0.9V is used as the supply voltage for the device, 1.62nm as graphene nanoribbon's width, 0.001 as doping concentrations of source and drain and 0% Line Edge Roughness. Simulations are performed for a period of 50ns and dynamic power is also measured for the same time.

In Figures (17-18) are shown the simulation results of all three technologies for different basic gates for channel lengths of 7nm and 10nm.



	MOSFET	CNTFET	GNRFET
Inverter	3.2577E-18	1.1361E-19	1.4125E-21
NAND	5.8756E-18	6.6055E-19	3.1993E-20
NOR	1.1298E-17	1.2214E-18	1.3955E-20
XOR	2.4663E-17	1.0546E-17	2.7620E-19

Figure 17. PDP Comparison for 7NM channel Length

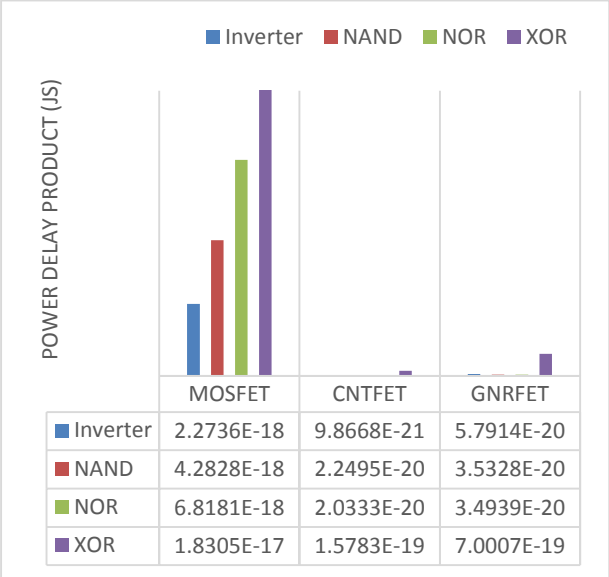


Figure 18. PDP Comparison for 10NM channel Length

From the Figures (17-18) of PDP of 7nm and 10nm channel length for MOSFET, CNTFET and GNRFET, it can be concluded that the PDP of CNTFET and GNRFET is lot less compared to that of MOSFET even though the MOSFET models used are based on FinFET structure. CNTFET and GNRFET operate faster than MOSFET and dissipate less power when compared to MOSFET resulting in lower PDP. This makes them more efficient than MOSFET devices.

Tables (1,2) give the simulation results of MOSFET, CNTFET and GNRFET for different basic gates for channel lengths of 32nm and 16nm. Simulation results from the Table (1,2) for the channel length of 16nm and 32nm indicate that EDP of CNTFET and GNRFET is lesser than that of MOSFET. This means that CNTFET and GNRFET consumes less energy to operate than MOSFET. As we decrease the channel length, delay of CNTFET and GNRFET decreases. On the other hand, their EDP also decreases significantly when compared to the EDP of MOSFET. This shows that CNTFET and GNRFET operate with minimal power consumption, making them suitable for low power applications.

Table 1. Comparison of MOSFET, CNTFET, and GNRFET with channel length 32nm

Logic Gate	MOSFET		CNTFET		GNRFET	
	Delay	EDP	Delay	EDP	Delay	EDP
Inverter	9.294 8E-12	1.022 1E-29	1.605 4E-12	1.080 2E-31	6.863 1E-13	8.650 3E-32
NAND2	1.625 0E-11	2.812 7E-29	2.377 3E-12	1.310 8E-31	1.792 1E-12	1.743 2E-31
NOR2	2.459 6E-11	6.044 0E-29	2.044 2E-12	9.978 0E-32	7.099 1E-13	2.959 7E-32
EXOR2	4.150 1E-11	7.351 8E-28	2.546 7E-12	7.564 2E-31	1.595 5E-12	6.013 8E-31

Table 2. Comparison of MOSFET, CNTFET, and GNRFET with channel length 16nm

Logic Gate	MOSFET		CNTFET		GNRFET	
	Delay	EDP	Delay	EDP	Delay	EDP
Inverter	9.2913 E-12	3.4270 E-30	1.662 8E-12	5.016 9E-32	3.784 7E-13	2.395 7E-32
NAND2	1.9016 E-11	1.2081 E-29	2.056 7E-12	4.936 4E-32	8.407 9E-13	2.069 1E-32
NOR2	3.7404 E-11	4.8876 E-29	1.679 8E-12	2.913 2E-32	8.821 3E-13	1.813 8E-33
EXOR2	5.7660 E-11	4.5380 E-28	2.596 3E-12	3.558 5E-31	1.412 2E-12	1.909 9E-30

4. Conclusion

There are various technologies like nanowire FET, single electron transistor, QCA and others which are currently undergoing lot of research that could replace the MOSFET technology, which is predicted to be reaching its scaling limits. In this paper, we looked at 2 different technologies both made of carbon material, CNTFET and GNRFET. Both these technologies showed lot of promises to replace the MOSFET technology because of their excellent electrical, thermal and physical properties. Among the properties of Carbon nanotubes, we studied, properties like pitch and number of carbon nanotubes can be used to easily modify the electrical conductivity of the CNTFET than chirality of the tube. Also, the effect of Line edge roughness, doping concentration and width of the GNR on performance of the GNRFET is analyzed. With the help of HSPICE simulations we were able to come up with numbers that suggest that CNTFET and GNRFET can be good candidates to replace MOSFET technology. Not only these devices operate faster but they also consume less power and also there is wide scope for future scaling. However, manufacturing techniques for these new devices still is not mature enough to be mass produced. Controlling the chirality during the carbon nanotube growth is still a challenge, likewise the graphene nanoribbon suffers from rough edges when cut from a graphene sheet which reduces the mean free path of the carriers. If some of the manufacturing challenges can be overcome, then either of these two technologies can be used to replace the MOSFET technology. In future, we would like extend the simulations to explore other technologies like NWFET and compare the performance with CNTFET and GNRFET. Also, we would like to study the performance of CNTFET and GNRFET for the channel length below 7nm.

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